

Bibliography

- [1] Hałgas S., "Algorytm lokalizacji uszkodzeń w nieliniowych układach elektronicznych", *Materiały XVI Seminarium z Podstaw Elektrotechniki i Teorii Obwodów*, SPETO'93, 247-253, 1993.
- [2] Hałgas S., "An algorithm for fault location and parameter identification of analog circuits based on interval arithmetics", *Proceedings of the XVI-th National Conference: Circuit Theory and Electronic Circuits*, KKTOiUE'93, 223-228, 1993.
- [3] Hałgas S., "An algorithm for fault location and parameter identification of analog circuits based on interval arithmetics", *Bulletin of the Polish Academy of Sciences, Technical Sciences*, Vol. 42, No. 1, 75-81, 1994.
- [4] Hałgas S., "Zastosowanie analizy wrażliwościowej w lokalizacji uszkodzeń", *Materiały XVII Seminarium z Podstaw Elektrotechniki i Teorii Obwodów*, SPETO'94, 359-364, 1994.
- [5] Hałgas S., "Wielowymuszeniowa metoda identyfikacji parametrów w elektronicznych układach prądu stałego", *Materiały XVIII Seminarium z Podstaw Elektrotechniki i Teorii Obwodów*, SPETO'95, 231-237, 1995.
- [6] Hałgas S., "Metoda słownikowa lokalizacji uszkodzeń i identyfikacji parametrów w układach nieliniowych", *Materiały XIX Seminarium z Podstaw Elektrotechniki i Teorii Obwodów*, SPETO'96, 413-416, 1996.
- [7] Hałgas S., "Algorytm lokalizacji uszkodzeń katastroficznych w układach diodowo-tranzystorowych prądu stałego", *Materiały XX Seminarium z Podstaw Elektrotechniki i Teorii Obwodów*, SPETO'97, 379-382, 1997.
- [8] Hałgas S., *Zastosowanie metod teorii obwodów w diagnostyce uszkodzeń statopräadowych układów elektronicznych*, Rozprawa doktorska, Łódź, 1998.

- [9] Hałgas S., "Nowa metoda lokalizacji uszkodzeń w tranzystorowych układach bipolarnych", *Materiały XXIII Międzynarodowej Konferencji z Podstaw Elektrotechniki i Teorii Obwodów*, IC-SPETO'2000, 297-300, 2000.
- [10] Hałgas S., "Algorytm wyznaczania potencjalnie stabilnych rozwiązań DC w bipolarnych układach tranzystorowych", *Materiały XXV Międzynarodowej Konferencji z Podstaw Elektrotechniki i Teorii Obwodów*, IC-SPETO'2002, (2), 385-388, 2002.
- [11] Hałgas S., Tadeusiewicz M., "Comparing some methods for finding all equilibrium states of transistor circuits", *Proceedings of IVth International Workshop: Computational Problems of Electrical Engineering*, CPEE'2002, 93-96, 2002.
- [12] Hałgas S., Tadeusiewicz M., "Tracing temperature characteristics in MOS-transistor circuits having multiple DC solutions", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES 2006, 609-612, 2006.
- [13] Hałgas S., "Metoda słownikowa wykrywania uszkodzeń parametrycznych w układach nieliniowych", *Materiały VI Krajowej Konferencji Elektroniki*, KKE'07, , (1), 119-124, 2007.
- [14] Hałgas S., Tadeusiewicz M., "Finding parametric characteristics in diode-transistor circuits", *Przegląd Elektrotechniczny - Konferencje*, (2), 20-23, 2007.
- [15] Hałgas S., "Multiple soft fault diagnosis of nonlinear circuits using the fault dictionary approach", *Bulletin of the Polish Academy of Sciences, Technical Sciences*, (56), 53-57, 2008.
- [16] Hałgas S., Tadeusiewicz M., "Analysis of CMOS circuits having multiple DC operating points", *Proceedings of 2010 International Workshop: Computational Problems of Electrical Engineering*, CPEE'2010, stron 4, 2010.
- [17] Hałgas S., Tadeusiewicz M., "Analysis of CMOS circuits having multiple DC operating points", *Przegląd Elektrotechniczny*, (5), 40-42, 2011.
- [18] Hałgas S., Tadeusiewicz M., "An algorithm for finding multiple DC operating points using the concept of restart homotopy", *Proceedings of joint conference Computational Problems of Electrical Engineering and Advanced Methods of the Theory of Electrical Engineering*, CPEE-AMTEE 2013, II-1, 2013.

- [19] Hałgas S., Tadeusiewicz M., "Improvement of the search method for parametric fault diagnosis of analog Integrated Circuits", *Proceedings of the 23rd International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2016, Łódź, Poland*, 359-362, 2016, DOI: 10.1109/MIXDES.2016.7529765.
- [20] Tadeusiewicz M., Hałgas S., "Continuation algorithms for solving nonlinear resistive circuits", *Proceedings of the XV-th National Conference: Circuit Theory and Electronic Circuits*, KKTOiUE'92, 42-47, 1992.
- [21] Tadeusiewicz M., Hałgas S., "DC analysis of nonlinear electronic circuits via homotopy approach", *Zeszyty Naukowe Politechniki Łódzkiej, Elektryka*, (87), 77-87, 1994.
- [22] Tadeusiewicz M., Hałgas S., "Usprawniony algorytm testu znaku wyznaczania wszystkich rozwiązań DC układów zawierających tranzystory MOS", *Materiały XX Seminarium z Podstaw Elektrotechniki i Teorii Obwodów*, SPETO'97, 399-402, 1997.
- [23] Tadeusiewicz M., Jagocki M., Hałgas S., "Improvement of the sign test for finding all the DC solutions of piecewise-linear circuits", *International Journal of Circuit Theory and Applications*, (26), 531-538, 1998.
- [24] Tadeusiewicz M., Hałgas S., "Finding all the DC solution of a certain class of piecewise-linear circuits", *Journal of Circuits, System and Signal Processing*, (18), 89-110, 1999.
- [25] Tadeusiewicz M., Hałgas S., "An effective algorithm for finding all equilibrium states of circuits containing Gummel-Poon modeled transistors", *Proceedings of the 6th International Conference on Mixed Design of Integrated Circuits and Systems*, MIXDES'99, 163-166, 1999.
- [26] Tadeusiewicz M., Hałgas S., "An effective algorithm for finding all the DC solution of MOS transistor circuits represented by original polynomial nonlinearities", *Proceedings of the European Conference on Circuit Theory and Design*, ECCTD'99, 467-470, 1999.
- [27] Tadeusiewicz M., Hałgas S., "Finding all the DC solution of the DC solutions of MOS transistor circuits described by original nonlinear equations", *Kwartalnik Elektroniki i Telekomunikacji*, (46), 281-297, 2000.

- [28] Tadeusiewicz M., Hałgas S., "An algorithm for finding all the DC solution of short-channel MOS transistor circuits", *Proceedings of the 7th IEEE International Conference on Electronics, Circuits, and Systems*, ICECS'2000, 924-927, 2000.
- [29] Tadeusiewicz M., Hałgas S., "An algorithm for soft fault diagnosis of DC circuits", *Proceedings of the 15th European Conference on Circuit Theory and Design*, ECCTD'01, (1), 245-248, 2001.
- [30] Tadeusiewicz M., Hałgas S., "Soft fault diagnosis of nonlinear DC circuits", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES'2001, 341-347, 2001.
- [31] Tadeusiewicz M., Hałgas S., "An improved algorithm for the analysis of MOS transistor circuits having multiple DC solutions", *Proceedings of XI International Symposium on Theoretical Electrical Engineering*, ISTET'2001, CDROM, stron 4, 2001.
- [32] Tadeusiewicz M., Hałgas S., "Wyznaczanie charakterystyk typu wejście-wyjście w nielinowych układach elektronicznych", *Materiały XXV Międzynarodowej Konferencji z Podstaw Elektrotechniki i Teorii Obwodów*, IC-SPETO'2002, (2), 203-206, 2002.
- [33] Tadeusiewicz M., Hałgas S., "Determining multi-valued input-output characteristics in the circuits containing bipolar transistors", *Proceedings of the 9th IEEE International Conference on Electronics, Circuits, and Systems*, ICECS'2002, 987-990, 2002.
- [34] Tadeusiewicz M., Hałgas S., Korzybski M., "An algorithm for soft-fault diagnosis of linear and nonlinear circuits", *IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications*, (49), 1648-1653, 2002.
- [35] Tadeusiewicz M., Halgas S., "An improved algorithm for finding all the DC solutions of MOS transistor circuits", *Kwartalnik Elektroniki i Telekomunikacji*, (49), 7-17, 2003.
- [36] Tadeusiewicz M., Hałgas S., "Zastosowanie funkcji W-Lamberta do wyznaczania charakterystyki przejściowej detektora AM", *Materiały XXVI Międzynarodowej Konferencji z Podstaw Elektrotechniki i Teorii Obwodów*, IC-SPETO'2003, (2), 279-282, 2003.

- [37] Tadeusiewicz M., Hałgas S., "DC analysis of circuits containing short-channel MOS transistors", *Proceedings of the 10th International Conference on Mixed Design of Integrated Circuits and Systems*, MIXDES'03, 421-426, 2003.
- [38] Tadeusiewicz M., Hałgas S., "Transient analysis of nonlinear dynamic circuits using a numerical-integration method", *Proceedings of XII International Symposium on Theoretical Electrical Engineering*, ISTET'2003, (1), 131-134, 2003.
- [39] Tadeusiewicz M., Hałgas S., "Tracing input-output characteristics in circuits containing the Gummel-Poon modeled transistors", *Proceedings of the European Conference on Circuit Theory and Design*, ECCTD'03, (1), 161-164, 2003.
- [40] Tadeusiewicz M., Hałgas S., "Short-channel MOS transistor circuits: finding all the DC solutions and input-output characteristics", *Kwartalnik Elektroniki i Telekomunikacji*, (49), 515-538, 2003.
- [41] Tadeusiewicz M., Hałgas S., "Computing input-output characteristics of circuits containing idealized diodes and transistors", *Proceedings of VIth International Workshop: Computational Problems of Electrical Engineering*, CPEE'2004, 50-53, 2004.
- [42] Tadeusiewicz M., Hałgas S., "An algorithm for the analysis of dynamic electronic circuits", *Proceedings of VIth International Workshop: Computational Problems of Electrical Engineering*, CPEE'2004, 221-224, 2004.
- [43] Tadeusiewicz M., Hałgas S., "Finding all the DC solutions of circuits containing idealized diodes and transistors", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES'2004, 51-54, 2004.
- [44] Tadeusiewicz M., Hałgas S., "Computing multivalued input-output characteristics in the circuits containing bipolar transistors", *IEEE Transactions on Circuits and Systems - I: Regular Papers*, (51), 1859-1867, 2004.
- [45] Tadeusiewicz M., Hałgas S., "Analiza staloprądowa układów zawierających tranzystory MOS z krótkim kanałem", *Elektronika - konstrukcje, technologie, zastosowania*, (11), 50-53, 2004.
- [46] Tadeusiewicz M., Hałgas S., "Transient analysis of nonlinear dynamic circuits using a numerical-integration method", *COMPEL: International Journal*

- for Computation and Mathematics in Electrical and Electronic Engineering*, (24), 707-719, 2005.
- [47] Tadeusiewicz M., Hałgas S., "Evaluation of the faulty parameters of analog circuits", *Proceedings of XIII International Symposium on Theoretical Electrical Engineering*, ISTET 2005, 384-387, 2005.
 - [48] Tadeusiewicz M., Hałgas S., Sidyk P., "Building and exploiting fault dictionary for transistor circuits diagnosis", *Proceedings of XIII International Symposium on Theoretical Electrical Engineering*, ISTET 2005, 388-391, 2005.
 - [49] Tadeusiewicz M., Pawlak K., Hałgas S., "DC analysis of diode transistor circuits", *Proceedings of XIII International Symposium on Theoretical Electrical Engineering*, ISTET 2005, 392-395, 2005.
 - [50] Tadeusiewicz M., Hałgas S., "Analysis of diode-transistor circuits having multiple DC solutions", *Proceedings of the European Conference on Circuit Theory and Design*, ECCTD 2005, (3), 39-42, 2005.
 - [51] Tadeusiewicz M., Hałgas S., "Multiple fault diagnosis in analogue circuits", *Proceedings of the European Conference on Circuit Theory and Design*, ECCTD 2005, (3), 205-208, 2005.
 - [52] Tadeusiewicz M., Hałgas S., "Tracing AM-detector transfer characteristics", *COMPEL: International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, (24), 1439-1449, 2005.
 - [53] Tadeusiewicz M., Hałgas S., "Diagnostyka układów elektronicznych z wielokrotnymi uszkodzeniami", *Materiały XXIX Międzynarodowej Konferencji z Podstaw Elektrotechniki i Teorii Obwodów*, IC-SPETO'2006, (2), 279-282, 2006.
 - [54] Tadeusiewicz M., Hałgas S., "Wyznaczanie charakterystyk temperaturowych w układach diodowo-tranzystorowych o wielu punktach równowagi", *Materiały V Krajowej Konferencji Elektroniki*, KKE'2006, (1), 63-68, 2006.
 - [55] Tadeusiewicz M., Hałgas S., "A method for the analysis of transistor circuits having multiple DC solutions", *International Journal of Electronics and Communications*, (AEÜ), (60), 582-589, 2006.
 - [56] Tadeusiewicz M., Hałgas S., "Finding all the DC solutions in circuits containing bipolar transistors", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES 2006, 361-364, 2006.

- [57] Tadeusiewicz M., Hałgas S., "An algorithm for multiple fault diagnosis in analogue circuits", *International Journal of Circuit Theory and Applications*, (34), 607-615, 2006.
- [58] Tadeusiewicz M., Hałgas S., Sidyk P., "Metoda wykrywania uszkodzeń parametrycznych w układach tranzystorowych", *Materiały VI Krajowej Konferencji Elektroniki*, KKE'07, (1), 113-118, 2007.
- [59] Tadeusiewicz M., Sidyk P., Hałgas S., "A method for multiple fault diagnosis in dynamic analogue circuits", *Proceedings of the European Conference on Circuit Theory and Design*, ECCTD 2007, 834-837, 2007.
- [60] Tadeusiewicz M., Hałgas S., "Finding all the DC solutions of transistor circuits with the thermal constraint", *Proceedings of the European Conference on Circuit Theory and Design*, ECCTD 2007, 982-985, 2007.
- [61] Tadeusiewicz M., Hałgas S., "Finding operating points of the diode-transistor circuits via homotopy approach", *Przegląd Elektrotechniczny - Konferencje*, (2), 69-72, 2007.
- [62] Tadeusiewicz M., Hałgas S., "Tracing temperature characteristics in diode-transistor circuits having multiple DC solutions", *Bulletin of the Polish Academy of Sciences, Technical Sciences*, (55), 317-323, 2007.
- [63] Tadeusiewicz M., Hałgas S., Sidyk P., "Metoda wykrywania uszkodzeń parametrycznych w układach tranzystorowych", *Elektronika - Konstrukcje, Technologie, Zastosowania*, (11), 31-33, 2007.
- [64] Tadeusiewicz M., Hałgas S., "Wyznaczanie statycznych charakterystyk w układach tranzystorowych z wykorzystaniem symulatora analizy dynamicznej SPICE", *Materiały VII Krajowej Konferencji Elektroniki*, KKE'08, (2), 349-354, 2008.
- [65] Tadeusiewicz M., Hałgas S., "Zastosowanie koncepcji homotopii do analizy DC układów tranzystorowych z uwzględnieniem zjawiska samonagrzewania", *Materiały VII Krajowej Konferencji Elektroniki*, KKE'08, (2), 361-366, 2008.
- [66] Tadeusiewicz M., Hałgas S., "Tracing some temperature characteristics in diode-transistor circuits having multiple DC solutions", *Proceedings of the 15th IEEE International Conference on Electronics, Circuits, and Systems*, ICECS'2008, 247-250, 2008.

- [67] Tadeusiewicz M., Hałgas S., "An efficient method for simulation of multiple catastrophic faults", *Proceedings of the 15th IEEE International Conference on Electronics, Circuits, and Systems*, ICECS'2008, 356-359, 2008.
- [68] Hałgas S., Tadeusiewicz M., "Multiple soft fault diagnosis of analogue electronic circuits", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES'08, 533-536, 2008.
- [69] Tadeusiewicz M., Hałgas S., "Wyznaczanie statycznych charakterystyk w układach tranzystorowych z wykorzystaniem symulatora analizy dynamicznej SPICE", *Elektronika - Konstrukcje, Technologie, Zastosowania*, (11), 170-173, 2008.
- [70] Tadeusiewicz M., Hałgas S., "Zastosowanie koncepcji homotopii do analizy DC układów tranzystorowych z uwzględnieniem zjawiska samonagrzewania", *Elektronika - Konstrukcje, Technologie, Zastosowania*, (11), 140-144, 2008.
- [71] Tadeusiewicz M., Hałgas S., "Analiza układów nieliniowych o wielu rozwiązańach DC", *Materiały VIII Krajowej Konferencji Elektroniki KKE'09*, 227-232, 2009.
- [72] Tadeusiewicz M., Hałgas S., "Analysis of transistor circuits having multiple DC solutions with the thermal constraint", *Proceedings of XV International Symposium on Theoretical Electrical Engineering, ISTEET'2009, Lubeck, Germany*, 45-48, 2009.
- [73] Tadeusiewicz M., Hałgas S., "Finding all the DC solutions of circuits containing diodes and bipolar transistors", *Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009, Łódź, Poland*, 433-437, 2009.
- [74] Tadeusiewicz M., Hałgas S., "Improved algorithm for computing all the DC operating points of diode-transistor circuits", *Proceedings of the 2009 European Conference on Circuit Theory and Design ECCTD'09, Antalya, Turkey*, 489-492, 2009.
- [75] Tadeusiewicz M., Hałgas S., "Multiple catastrophic fault diagnosis of linear circuits considering the component tolerances", *Proceedings of the 2009 European Conference on Circuit Theory and Design ECCTD'09, Antalya, Turkey*, 647-650, 2009.

- [76] Tadeusiewicz M., Hałgas S., "Contraction and elimination methods for finding multiple DC solutions of bipolar circuits", *Przegląd Elektrotechniczny*, (11), 149-152, 2009.
- [77] Tadeusiewicz M., Hałgas S., "Contraction and elimination methods for finding multiple DC solutions of bipolar circuits", *Proceedings of VIth International Workshop: Computational Problems of Electrical Engineering*, CPEE'2009, stron 3, 2009.
- [78] Tadeusiewicz M., Hałgas S., "Finding all the DC solutions of circuits containing diodes and bipolar transistors", *Elektronika - Konstrukcje, Technologie, Zastosowania*, (12), 39-42, 2009.
- [79] Tadeusiewicz M., Hałgas S., "Contraction and elimination methods for finding multiple DC solutions of bipolar circuits", *Przegląd Elektrotechniczny*, (1), 11-13, 2010.
- [80] Tadeusiewicz M., Hałgas S., "A method for fast simulation of multiple catastrophic faults in analogue circuits", *International Journal of Circuit Theory and Applications*, (38), 275-290, 2010.
- [81] Tadeusiewicz M., Hałgas S., "Soft fault diagnosis of nonlinear analog circuits using the continuation approach", *International Symposium on Nonlinear Theory and its Applications (NOLTA2010)*, 366-369, 2010.
- [82] Tadeusiewicz M., Hałgas S., "A fast method for tracing multi-valued characteristics in nonlinear circuits", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES'2010, 177-180, 2010.
- [83] Tadeusiewicz M., Hałgas S., "A simple approach to the analysis of nonlinear circuits having multiple DC solutions", *Proceedings of 2010 International Workshop: Computational Problems of Electrical Engineering*, CPEE'2010, stron 4, 2010.
- [84] Tadeusiewicz M., Hałgas S., "Szybka metoda wyznaczania wielowartościowych charakterystyk w układach nieliniowych", *Elektronika - Konstrukcje, Technologie, Zastosowania*, (12), 33-35, 2010.
- [85] Tadeusiewicz M., Hałgas S., "Some contraction methods for locating and finding all the DC operating points of diode-transistor circuits", *International Journal of Electronics and Telecommunications*, (56), 331-338, 2010.

- [86] Tadeusiewicz M., Hałgas S., "Diagnostyka układów nieliniowych z uwzględnieniem tolerancji elementów", *Materiały X Krajowej Konferencji Elektroniki KKE'11*, 890-895, 2011.
- [87] Tadeusiewicz M., Hałgas S., "Analysis of transistor circuits having multiple DC solutions with the thermal constraint", *COMPEL: International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, (30), 1351-1363, 2011.
- [88] Tadeusiewicz M., Hałgas S., "Multiple soft fault diagnosis of nonlinear DC circuits considering component tolerances", *Metrology and Measurement Systems*, (18), 349-360, 2011.
- [89] Tadeusiewicz M., Hałgas S., "A contraction method for locating all the DC solutions of circuits containing bipolar transistors", *Circuits, Systems, and Signal Processing*, (31), 1159-1166, 2012.
- [90] Tadeusiewicz M., Hałgas S., "Multiple soft fault diagnosis of nonlinear circuits using the continuation method", *Journal of Electronic Testing: Theory and Applications*, (28), 487-493, 2012.
- [91] Tadeusiewicz M., Hałgas S., "Analysis of BJT circuits having multiple DC solutions using deflation technique", *Proceedings of the International Conference on Signals and Electronic Systems*, ICSES'2012, stron 4, 2012, DOI:10.1109/ICSES.2012.6382253.
- [92] Tadeusiewicz M., Hałgas S., Korzybski M., "Multiple catastrophic fault diagnosis of analog circuits considering the component tolerances", *International Journal of Circuit Theory and Applications*, (40), 1041-1052, 2012.
- [93] Tadeusiewicz M., Hałgas S., "A method for finding multiple DC operating points of short channel CMOS circuits", *Circuits, Systems, and Signal Processing*, (32), 2457-2468, 2013.
- [94] Tadeusiewicz M., Hałgas S., "Lokalizacja i identyfikacja uszkodzeń parametrycznych w układach analogowych", *Materiały XXXVI Międzynarodowej Konferencji z Podstaw Elektrotechniki i Teorii Obwodów*, IC-SPETO'2013, 73-74, 2013.
- [95] Tadeusiewicz M., Hałgas S., "Multiple soft fault diagnosis of analog circuits using restart homotopy method", *Proceedings of 2013 International Symposium on Theoretical Electrical Engineering*, ISTET'2013, Pilsen, Czech Republic, 24th - 26th June 2013, II-15 - I-16, 2013.

- [96] Tadeusiewicz M., Hałgas S., "Multiple soft fault diagnosis of analog circuits using restart homotopy method", *Elektronika - Konstrukcje, Technologie, Zastosowania*, (12), 87-91, 2013.
- [97] Tadeusiewicz M., Hałgas S., "Global and local parametric diagnosis of analog short-channel CMOS circuits using homotopy-simplicial algorithm", *International Journal of Circuit Theory and Applications*, (42), 1051-1068, 2014.
- [98] Tadeusiewicz M., Hałgas S., "Numerical analysis of direct current circuits containing bipolar and metal oxide semiconductor transistors", *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, (27), 935-948, 2014, DOI: 10.1002/jnm.1989.
- [99] Tadeusiewicz M., Hałgas S., "Multiple soft fault diagnosis of BJT circuits", *Metrology and Measurement Systems*, (21), 663-674, 2014.
- [100] Tadeusiewicz M., Kuczyński A., Hałgas S., "Catastrophic fault diagnosis of a certain class of nonlinear analog circuits", *Circuits, Systems, and Signal Processing*, (34), 353-375, 2015, DOI 10.1007/s00034-014-9857-7.
- [101] Tadeusiewicz M., Hałgas S., Kuczyński A., "New aspects of fault diagnosis of nonlinear analog circuits", *International Journal of Electronics and Telecommunications*, (61), 83-93, 2015, DOI: 10.1515/eletel-2015-0011.
- [102] Tadeusiewicz M., Hałgas S., "New approach to multiple soft fault diagnosis of analog BJT and CMOS circuits", *IEEE Transactions on Instrumentation and Measurement*, (64), 2688-2695, 2015, DOI: 10.1109/TIM.2015.242171.
- [103] Tadeusiewicz M., Kuczyński A., Hałgas S., "Spot defect diagnosis in analog nonlinear circuits with possible multiple operating points", *Journal of Electronic Testing: Theory and Applications*, (31), 491-502, 2015.
- [104] Tadeusiewicz M., Hałgas S., "Multiple soft fault diagnosis of DC analog CMOS circuits designed in nanometer technology", *Analog Integrated Circuits and Signal Processing*, (88), 65-77, 2016, DOI 10.1007/s10470-016-0752-y.
- [105] Tadeusiewicz M., Hałgas S., "Diagnosis of spot short defects in analog circuits considering the thermal behavior of the chip", *Metrology and Measurement Systems*, (23), 239-250, 2016, DOI: 10.1515/mms-2016-0023.
- [106] Tadeusiewicz M., Hałgas S., "A systematic method for arranging diagnostic tests in linear analog DC and AC circuits", *Journal of Electronic Testing*:

- Theory and Applications*, (33), 147-156, 2017, DOI 10.1007/s10836-017-5650-4.
- [107] Tadeusiewicz M., Hałgas S., "Diagnosis of a soft short and local variations of parameters occurring simultaneously in analog CMOS circuits", *Microelectronics Reliability*, (72), 90-97, 2017, DOI 10.1016/j.microrel.2017.03.025.
 - [108] Tadeusiewicz M., Hałgas S., "A method for local parametric fault diagnosis of a broad class of analog integrated circuits", *IEEE Transactions on Instrumentation and Measurement*, (67), 328-337, 2018, DOI: 10.1109/TIM.2017.2775438.
 - [109] Tadeusiewicz M., Hałgas S., "A fault verification method for testing of analogue electronic circuits", *Metrology and Measurement Systems*, (25), 331-346, 2018, DOI: 10.24425/119558.
 - [110] Tadeusiewicz M., Hałgas S., "A method for multiple soft fault diagnosis of linear analog circuits", *Measurement*, (131), 714-722, 2019, DOI: 10.1016/j.measurement.2018.09.001.
 - [111] Tadeusiewicz M., Hałgas S., "A method for fault diagnosis of nonlinear circuits", *COMPEL - The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, (38), 1770-1781, 2019, DOI: 10.1108/COMPEL-03-2019-0101.
 - [112] Tadeusiewicz M., Hałgas S., "Soft fault diagnosis of linear circuits with the special attention paid to the circuits containing current conveyors", *AEU - International Journal of Electronics and Communications*, (115), 153036, 2020, DOI: 10.1016/j.aeue.2019.153036.
 - [113] Tadeusiewicz M., Hałgas S., "Soft fault diagnosis of non-linear circuits having multiple DC solutions", *IET Circuits, Devices & Systems*, (14), 1220-1227, 2020, DOI:10.1049/iet-cds.2020.0197.
 - [114] Tadeusiewicz M., Hałgas S., "A method for diagnosing soft short and open faults in distributed parameter multiconductor transmission lines", *Electronics*, 10(1), 35, 2021, DOI:10.3390/electronics10010035.
 - [115] Tadeusiewicz M., Hałgas S., "Parametric fault diagnosis of very high-frequency circuits containing distributed parameter transmission lines", *Electronics*, 10(5), 550, 2021, DOI:10.3390/electronics10050550.

- [116] Tadeusiewicz M., Hałgas S., "A Method for Parametric and Catastrophic Fault Diagnosis of Analog Linear Circuits", *IEEE Access*, 10, pp. 27002-27013, 2022, doi: 10.1109/ACCESS.2022.3157647.